What Is Claimed Is:

1. A method for matching electrical characteristics of components of a semiconductor integrated circuit, comprising the steps of:

dividing at least a first component and a second component of a semiconductor integrated circuit into a plurality of unit cells, wherein the first component and second component are components whose electrical properties are to be precisely or proportionally matched, and wherein each unit cell is the same size; and

uniformly distributing the plurality of unit cells for the first and second components in an array.

2. The method of claim 1, further comprising placing a plurality of dummy cells in the array, wherein each dummy cell is the same size as a unit cell.

3. The method of claim 2, wherein the dummy cells are placed near an outer perimeter of the array.

4. The method of claim 1, wherein the step of uniformly distributing the plurality of unit cells for the first and second components in an array comprises uniformly distributing unit cells of the first component in the array

and evenly distributing unit cells of the second component around the unit cells of the first component.

5. The method of claim 1, wherein dividing at least a first component and a second component of a semiconductor integrated circuit into a plurality of unit cells, comprises:

defining a full-unit cell that includes a plurality of sub-elements, wherein each sub-element is used for forming a component;

defining a size of sub-unit cell having a same layout area as the full-unit cell, wherein at least one or more of the sub-elements are dummy elements; and

determining a number full-unit cells and sub-unit cells to be used for forming the first component and the second component.

6. The method of claim 5, a size of the sub-unit cell is defined based on an area ratio between the first component and the second component.

7. The method of claim 6, wherein the area ratio is selected to obtain a resistance ratio, inductance ratio, capacitance ratio, current ratio, or voltage ratio.

8. The method of claim 1, wherein the first and second components are semiconductor transistors, resistors, capacitors, or inductors.

9. The method of claim 1, wherein the semiconductor integrated circuit is a differential amplifier, a reference current generator, a reference voltage generator, an analog-to-digital converter, a digital-to-analog converter, or a regulator.

10. A method for matching electrical characteristics of components of a semiconductor integrated circuit, comprising the steps of:

determining components of a semiconductor integrated circuit whose electrical characteristics are to be matched;

defining a size of a unit cell for the components;

forming each of the components using one of more unit cells;

defining an array comprising a plurality of cell lots for receiving unit cells;

uniformly distributing all unit cells of the components in the array; and

placing a dummy cell in each cell lot of the array not occupied by a unit cell.

11. The method of claim 10, wherein determining components of a semiconductor integrated circuit whose electrical characteristics are to be matched comprises determining the components whose electrical properties should be tracked to maintain a resistance ratio, an inductance ratio, a capacitance ratio, a current ratio, or voltage ratio.

12. The method of claim 10, wherein defining a size of a unit cell for the components comprises determining a number of sub-elements included in the unit cell.

13. The method of claim 10, wherein defining an array comprising a plurality of cell lots for receiving unit cells comprises defining an array structure having a plurality of cell lots disposed in rows and columns.

14. The method of claim 10, wherein uniformly distributing all unit cells of the components in the array comprises:

distributing all unit cells of a first component uniformly and symmetrically in the array; and

distributing all unit cells of a second component

uniformly and symmetrically relative to the locations of the unit cells of the first components in the array.

15. The method of claim 10, wherein uniformly distributing all unit cells of the components in the array comprises placing the unit cells in cell lots substantially in and around a central region of the array.

16. The method of claim 15, wherein placing a dummy cell in each cell lot of the array not occupied by a unit cell comprises placing dummy cells in cell lots adjacent a perimeter of the array.

17. A method for matching electrical characteristics of components of a semiconductor integrated circuit, comprising the steps of:

determining components of a semiconductor integrated circuit whose electrical characteristics are to be matched;

defining a unit cell for the components, wherein the unit cell comprises a plurality of sub-elements and wherein the unit cell has a layout area;

defining a sub-unit cell for the components based on the unit cell, wherein the sub-unit cell has the same number of sub-elements and layout area of the unit cell,

wherein one or more of the sub-elements of the sub-unit cell are dummy elements;

forming each component using one of more unit cells or one or more sub-unit cells;

defining an array comprising a plurality of cell lots for receiving unit cells or sub-unit cells;

uniformly distributing all unit cells and sub-unit cells of the components in the array; and

placing a dummy cell in each cell lot of the array not occupied by a unit cell or sub-unit cell.

18. The method of claim 17, wherein determining components of a semiconductor integrated circuit whose electrical characteristics are to be matched comprises determining the components whose electrical properties should be tracked to maintain a resistance ratio, an inductance ratio, a capacitance ratio, a current ratio, or voltage ratio.

19. The method of claim 17, wherein defining an array comprising a plurality of cell lots comprises defining an array structure having a plurality of cell lots disposed in rows and columns.

20. The method of claim 17, wherein uniformly distributing all unit cells and sub-unit cells of the components in the array comprises:

distributing all unit cells of a first component uniformly and symmetrically in the array; and

distributing all unit cells of a second component uniformly and symmetrically relative to the locations of the unit cells of the first components in the array.

21. The method of claim 17, wherein uniformly distributing all unit cells and sub-unit cells of the components in the array comprises evenly distributing the cell lots of unit cells and sub-unit cells substantially in and around a central region of the array.

22. The method of claim 21, wherein placing a dummy cell in each cell lot of the array not occupied by a unit cell or sub-unit cells comprises placing dummy cells in cell lots adjacent a perimeter of the array.

23. A semiconductor integrated circuit chip, comprising:

a circuit, wherein the circuit comprises a plurality of components that are divided into a plurality of unit

cells, wherein the circuit further comprises an array structure and wherein the unit cells are uniformly distributed in the array structure.

24. The semiconductor integrated circuit chip of claim 23, wherein the unit cells are associated with at least a first component and a second component whose electrical properties are to be precisely or proportionally matched.

25. The semiconductor integrated circuit chip of claim 23, wherein the array structure further comprises a plurality of dummy cells.

26. The semiconductor integrated circuit chip of claim 25, wherein each unit cell is the same size and wherein each dummy cell is the same size as the unit cells.

27. The semiconductor integrated circuit chip of claim 25, wherein the dummy cells are placed near an outer perimeter of the array structure.

28. The semiconductor integrated circuit chip of claim 24, wherein the unit cells for the first component

are evenly distributed in the array structure and wherein the unit cells of the second component are evenly distributed around the unit cells of the first component.

29. The semiconductor integrated circuit chip of claim 23, wherein the unit cells comprise full-unit cells and sub-unit cells, wherein each full-unit cell comprises a plurality of sub-elements that are used for forming a circuit component, and wherein each sub-unit cell comprises a same number of sub-elements as each full-unit cell, wherein one or more of the sub-elements of each sub-unit cell are dummy elements.

30. The semiconductor integrated circuit chip of claim 29, wherein one or more sub-unit cells are used for forming circuit components having different area ratios.

31. The semiconductor integrated circuit chip of claim 30, wherein different area ratios are selected to obtain a resistance ratio, inductance ratio, capacitance ratio, current ratio, voltage ratio, transistor width ratio, or other device size ratios.

32. The semiconductor integrated circuit chip of claim 23, wherein the circuit components are semiconductor transistors, resistors, capacitors, or inductors.

33. The semiconductor integrated circuit chip of claim 23, wherein the circuit is a differential amplifier, a reference current generator, a reference voltage generator, an analog-to-digital converter, a digital-to-analog converter, or a regulator.